ABSTRACT OF THE DISCLOSURE

Two reference signals are applied to an RC calibration circuit, which utilizes programmable resistors and switched capacitor resistors in parallel at the inputs of a differential amplifier with feedback capacitors, for the first cycle and then the two reference signals are swapped for the successive cycle. The circuit inherent DC offset is cancelled by these two successive cycles. The time duration when the difference of the differential amplifier outputs in the calibration circuit starts to reverse ramping direction and the time when the difference crosses zero is counted in terms of reference clock cycles by a binary counter. The binary count is used to select the capacitance of the capacitor arrays in an RC filter for time constant calibration. This calibration circuit provides the flexibility for various reference clock rates by adjusting the programmable resistors. By tuning the same programmable resistors, this calibration circuit in addition provides the capability to changing the cut-off frequency of an RC filter circuit to another predetermined value.

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